Failure Analysis (FA) Introduction

(IC Failure Mode)
Failure Mode

Structure of conventional package

- gold wire
- leadframe
- EMC
- die-pad

Failure Classification

Physical Failure (Structure)
- Popcorn
- Delamination
- Crack (Package/Die)

Electrical Failure (Connection)
- Open
- Short
- Leakage
- Function

In-Process Failure (Production)
- Front-end (before molding)
- Back-end (After molding)
- Testing (FT/Burn-in)

Reliability Failure (Qualification)
- Temperature
- Humidity
- Pressure
- Voltage
Failure Mechanism

1. Moisture absorption (L-1: 85°C/85%RH) (L-3: 30°C/60%RH)
2. Moisture vaporization during heating (Reflow, 235°C/10s)
3. Vapor force separating (delamination)
4. Popcorn forming (package crack) (collapsed void)
TQFP package (bottom popcorn)  FBGA package (top popcorn)
Delamination (離裂)

1. Die surface (EMC/chip)
2. Leadframe (EMC/leadframe)
3. Die Attach (chip/pad)
4. Pad bottom (pad/EMC)

Delamination (離裂)
Failure Mode

Crack (破裂)

EMC Crack (膠體破裂)

Die Crack (晶片破裂)

Failure Mode

leadframe

gold wire

chip

die-pad

EMC

crack

crack

EMC Crack (膠體破裂)

Die Crack (晶片破裂)
<table>
<thead>
<tr>
<th>No.</th>
<th>Package Crack Type</th>
<th>Shape</th>
<th>Problems</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Package rear-surface crack</td>
<td><img src="image1" alt="Diagram" /></td>
<td>. Moisture resistivity degradation (least degradation)</td>
</tr>
<tr>
<td>2</td>
<td>Package side crack</td>
<td><img src="image2" alt="Diagram" /></td>
<td>. Moisture resistivity degradation (small degradation)</td>
</tr>
</tbody>
</table>
| 3   | Crack intersecting a bounding wire | ![Diagram](image3) | . Wire damage, open  
. Moisture resistivity degradation |
| 4   | Package top-surface crack          | ![Diagram](image4) | . Wire damage, open  
. Wire bond peeled off  
. Moisture resistivity degradation |
Wiring Bondability (TSOP/BGA)

- Shift bonding (short/leakage, W/B)
- Ball lifted (open, W/B)
- Ball over-bonding (short, W/B)
Wiring Bondability (TSOP/BGA)

- Ball neck broken (W/B)
- Ball neck crack (W/B)
- Heel broken (open, W/B)
- Heel broken (open, W/B)
Inner Lead Bondability (TCP/COF)

- No bonding (open, ILB)
- Poor bonding (open, ILB)
- Thin bump (open, ILB)
- Thin lead (open, ILB)
Inner Lead Bondability (TCP/COF)

- Alloy bubble (short, ILB)
- IL shifted (short, ILB)
- Metal bridged (short, ILB)
- Bump crush (short, ILB)
**Bondability (Bonding Force)**

(function -> Leakage -> Short)

After crating testing
KNO3 solution etching
Remove gold-ball bonding
Inspect Al-pad

- Normal bondability

- SiO2 layer is damaged
2nd Bonding Broken
Open Failure

**Failure Mode**

- **Inner wire neck broken**
- **Foreign insulator stuck on lead**
- **Chip damaged to impact the wire**
- **Pad contamination by Auger Spectrum**

*Images and data plots are not readable due to the nature of the images.*
Open Failure

**TSOP II 54L LOC**
(in-process open failed)

Open bonding is not easily detected by XRM. However, after EMC decapsulation, 2nd bonding lifted is exposed by optical microscope.

**PLCC 32L**
(Reflowing open failed)

Open bonding is not easily detected by XRM. Bonding lifted is exposed by SEM.
Open Failure

Bending Test

- Output Y41
- Tape
- SEM found concave and micro-crack (1800x)

DC test open (Fail)

Vibration Test

- Open position
- TFT Panel
- ACF area
- SEM observed output lead broken (2000x)

Tung-Bao Lu
Open Failure

TCP Product
Inner Lead Bonding Broken

TCP Product
Resin Cause Broken

TCP Product
Inner Lead Peeling
Short Failure

Over-compressed bonding

Split epoxy between leadframe

Shifted bonding

Chip circuit burn out
**Short Failure**

- **Wire lay on substrate finger to short**
- **Sn whisker to connect two pins**
- **After PCT tests, solder growth**
- **Unloading from PCB, solder bridged**
One Model for Whisker Growth Mechanism

1. Substrate Elements (Cu, Zn, etc.) Diffuse into Sn Along Grain Boundaries.
2. Intermetallic Compound (IMC) may form preferentially in Grain Boundaries
3. As a Result, Stress Builds in Sn Layer (Compressive Stress)
4. To Relieve Stress, Whiskers EXTRUDE thru Ruptures in Sn Oxide
Failure Mode

**Short Failure**

- Sn over-plating to lead short on tape
- Needle-like Sn grow to short while bonding
- Chip scratched to cause circuit short
- Au pad bubble to short while bonding
Leakage Failure

- IC Circuit burn-out
- Corner die crack
- Die crack
  Top Temperature = 35.0°C
- Corner Chipping
Assembled Related – Machine/Man Damaged

- Corner chipping
- Side chipping
- Chip surface scratch
Assembled Related – Environment (Particle Damaged)

Particle damaged (~20um)

Particle damaged (~10um)
ESD Cases of Driver ICs

D-company, EOS/ESD wiring burn-out to short

H-company, internal burn-out to short, ESD under pad

(靜電防護元件~保險絲)
### Difference between ESD and EOS

<table>
<thead>
<tr>
<th><strong>ESD = ElectroStatic Discharge (ESD)</strong></th>
<th><strong>(EOS)</strong> <strong>EOS = Electrical Over Stress</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Appearance of damage (tendency)</strong></td>
<td>The location of damage is very small and cannot be identified by visually examining the semiconductor chip</td>
</tr>
<tr>
<td></td>
<td>If the energy of EOS is large of damage, such as breaks in wiring on the chip due to melting, discoloration, and burning of the package, can be recognized. If the energy is small, it is difficult to distinguish damage caused by EOS from that caused by ESD</td>
</tr>
<tr>
<td><strong>Process of failure</strong></td>
<td>Electric charge damages the IC chip of semiconductor device when it discharges through the device</td>
</tr>
<tr>
<td></td>
<td>A semiconductor device is damaged by application of an overvoltage or overcurrent while the device is operating (while the characteristics of the device are being used by the user)</td>
</tr>
<tr>
<td><strong>Cause of failure</strong></td>
<td>Discharge due to contact of a charged body with the pins of a semiconductor device or discharge of an electric charge that takes place in the device itself because of friction or other causes</td>
</tr>
<tr>
<td></td>
<td>Generation of Latch-up, surge due to turning power on or off and measuring instruments on or off, short-circuit of the load, solder chips, and patterns short-circuit by metallic foreign objects.</td>
</tr>
<tr>
<td><strong>Photograph of chip</strong></td>
<td><img src="image1" alt="Chip Photograph" /></td>
</tr>
</tbody>
</table>

Source: NEC information (1997, Guide to prevent damage for semiconductor devices by electrostatic discharge (ESD))
Major Mode of Damages by ESD

(1) Damage to oxide film
- Gate film is only 10nm
- Thin is easy

(2) Junction destruction
- Reverse bias
- Current concentration
- Shallow is easy

(3) Melting of wiring film
- Thermal destruction
- ESD (fine Al wiring is melted)
- EOS (coarse Al wiring)
- Thin is easy

Source: NEC information (1997, Guide to prevent damage for semiconductor devices by electrostatic discharge (ESD))